Chapter 6
The Field Effect Transistor

BJTs

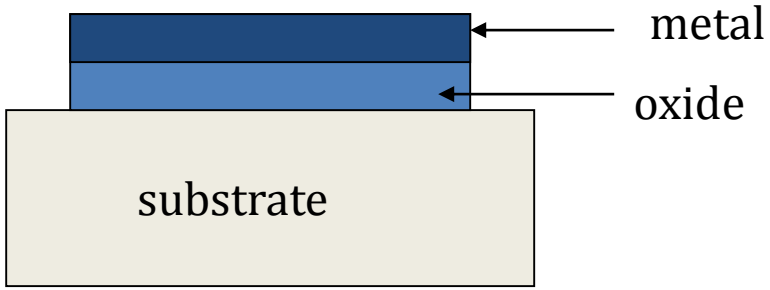
- Three different currents in the device: I_C, I_B and I_E
- Consume a lot of power
- Large size device

MOSFETs

- Mostly widely used today
- Low power
- Very small device (nm)
- Simple manufacturing process
- Only 1 current, I_D

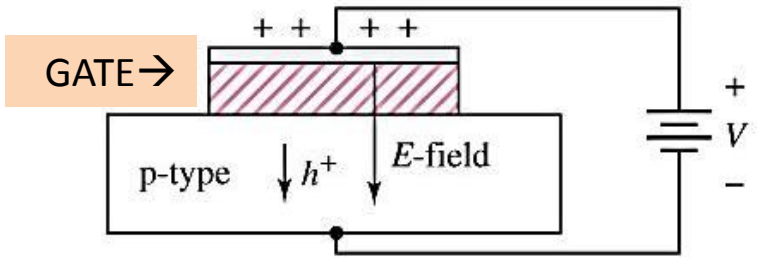
MOS Field Effect Transistor

- In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current.
- The phenomenon is called the **field effect.**
- The basic transistor principle is that the voltage between two terminals, provides the electric field, and controls the current through the third terminal.



Two-Terminal MOS Structure

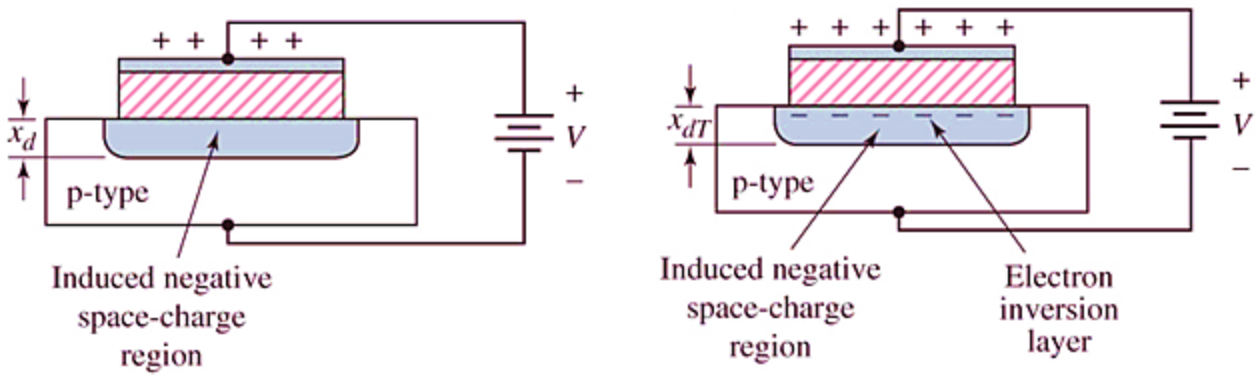
- A MOS capacitor with a p-type semiconductor substrate: the top metal terminal, called the **gate**, is at a positive voltage with respect to the substrate.
- A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction
- If the electric field penetrates the semiconductor, holes in the p-type material will experience a force away from the oxide-semiconductor interface.



(a)

Two-Terminal MOS Structure

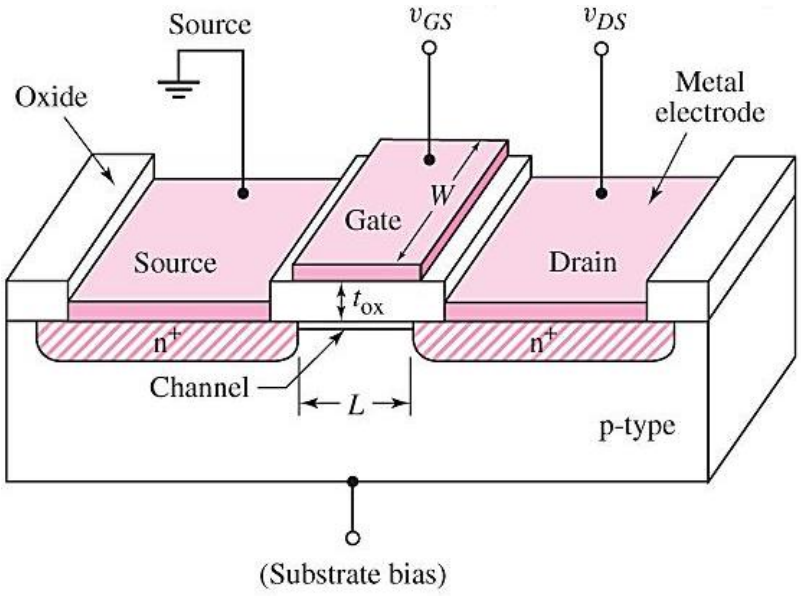
- As the holes are pushed away from the interface, a negative space-charge region is created.
- This region of minority carrier electrons is called an **electron inversion layer**.
- The magnitude of the charge in the inversion layer is a function of the applied gate voltage, hence the larger voltage is applied, the wider it becomes



NMOS Enhancement Mode

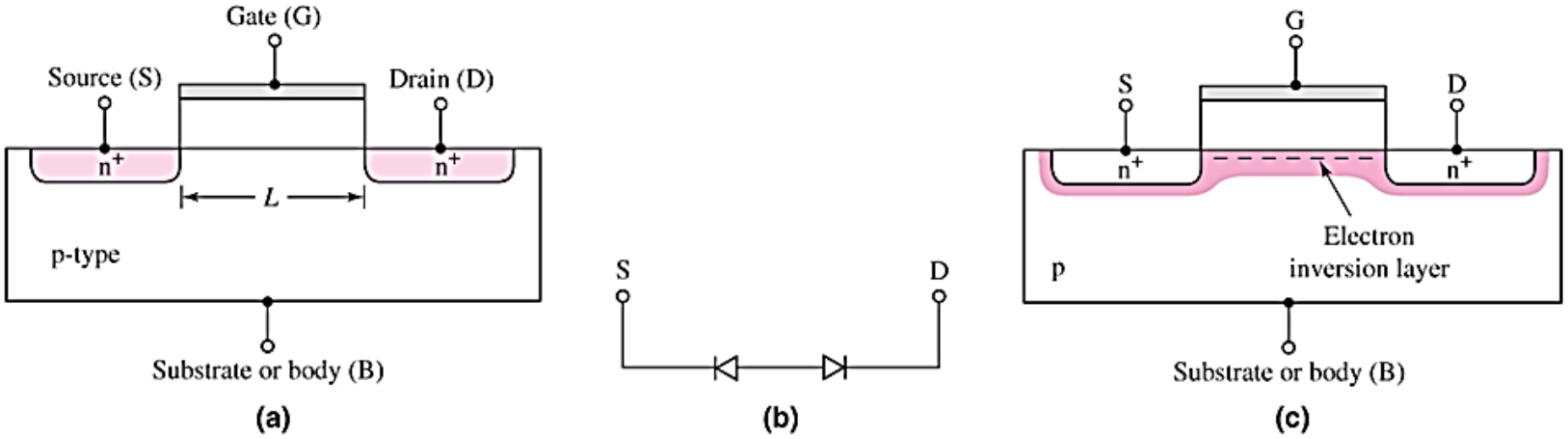
- **Transistor Structure**

- The gate, oxide, and p-type substrate are the same as those of a MOS capacitor.
- There are two *n*-regions, called the **source** and **drain** terminal.
- The current in a MOSFET is the result of the flow of charge in the inversion layer, called the **channel region**, adjacent to the oxide-semiconductor interface.



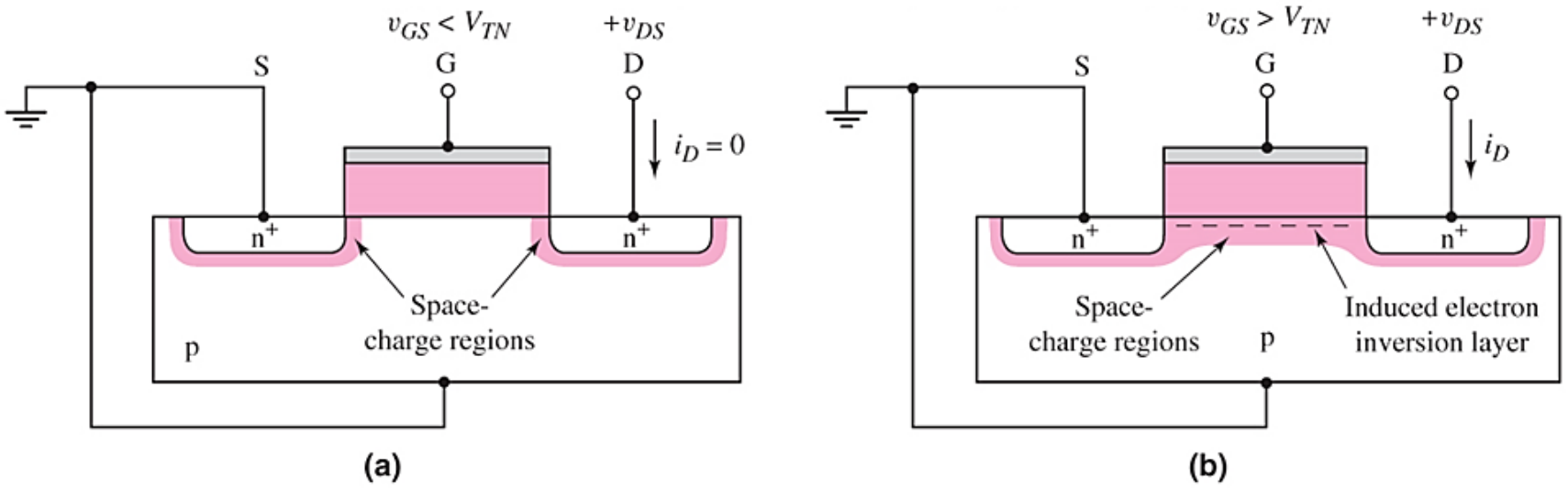
NMOS Enhancement Mode

- If a large enough positive voltage gate voltage is applied, an electron inversion layer connects the n-source to the n-drain.
- A current can then be generated between the source and drain terminals.
- Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement mode MOSFET.**
- Since the carriers in the inversion layer are electrons, this device is called an **n-channel MOSFET (NMOS).**

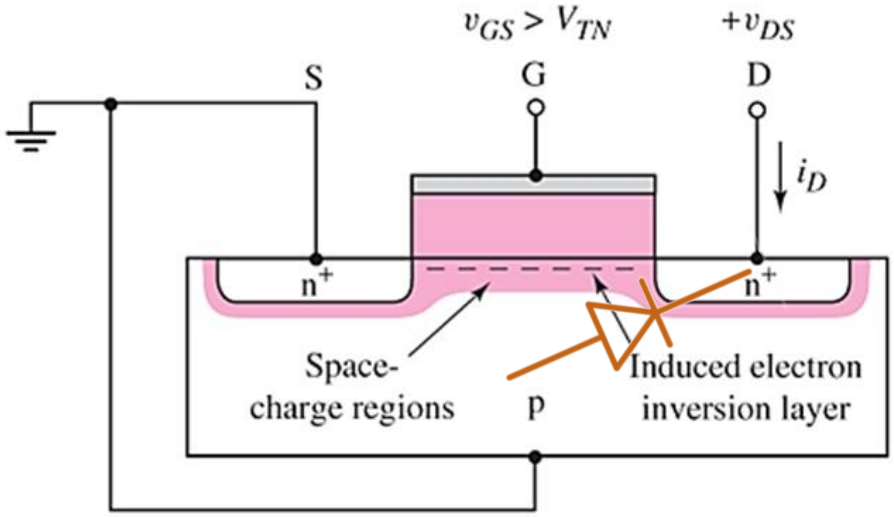


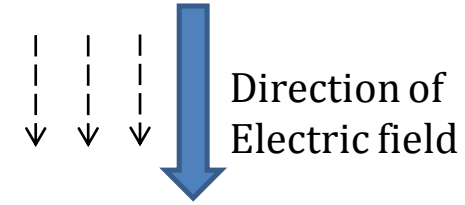
Ideal MOSFET Current-Voltage Characteristics – NMOS Device

- The **threshold voltage** of the n-channel MOSFET, denoted as V_{TH} *or* $V_{TN,}$ is defined as the applied gate voltage needed to create an inversion charge.
- If the $V_{GS} < V_{TN,}$ the current in the device is essentially zero.
- If the $V_{GS} > V_{TN,}$ a drain-to-source current, I_D is generated as an induced electron inversion layer / channel is created



Ideal MOSFET Current-Voltage Characteristics – NMOS Device



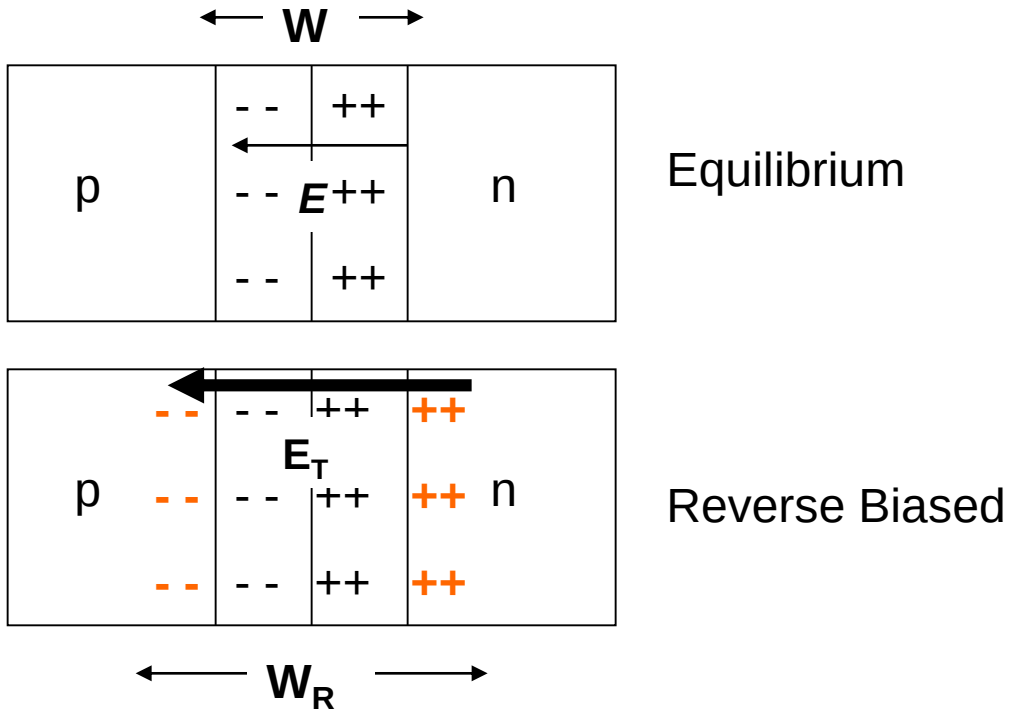


holes experience force same direction of electric field, leaving an electron inversion layer

- A positive but small drain voltage, V_{DS} creates a reverse-biased drain-to-substrate pn junction, depletion region width increases
- At the drain end, the inversion layer *bridges* the depletion region, providing a path for the current to flow.
- So current flows through the channel region, not through a pn junction.

Reverse-Biased pn Junction

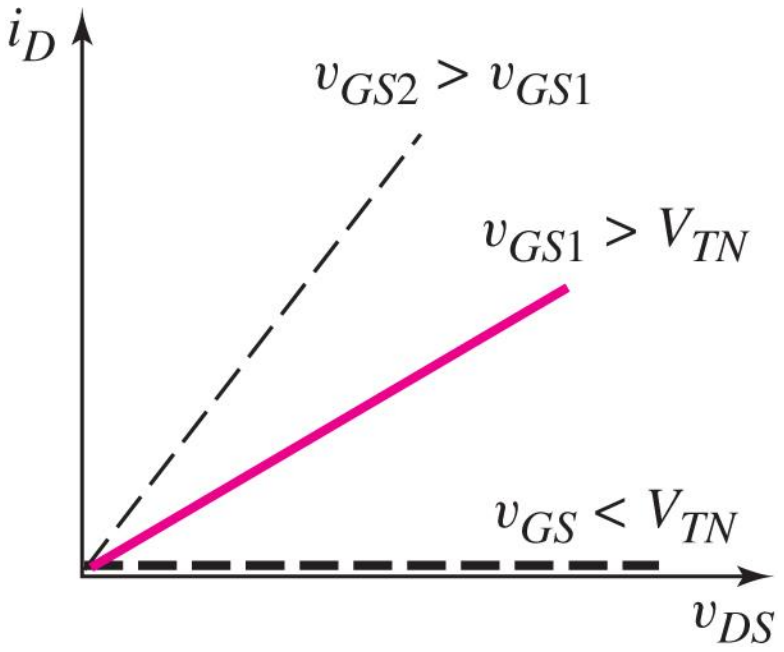
- There is an increase of the electric field in the depletion region, the number of charges increases too since the width of the depletion increases.



Ideal MOSFET Current-Voltage Characteristics – NMOS Device - Small value of V_{DS}

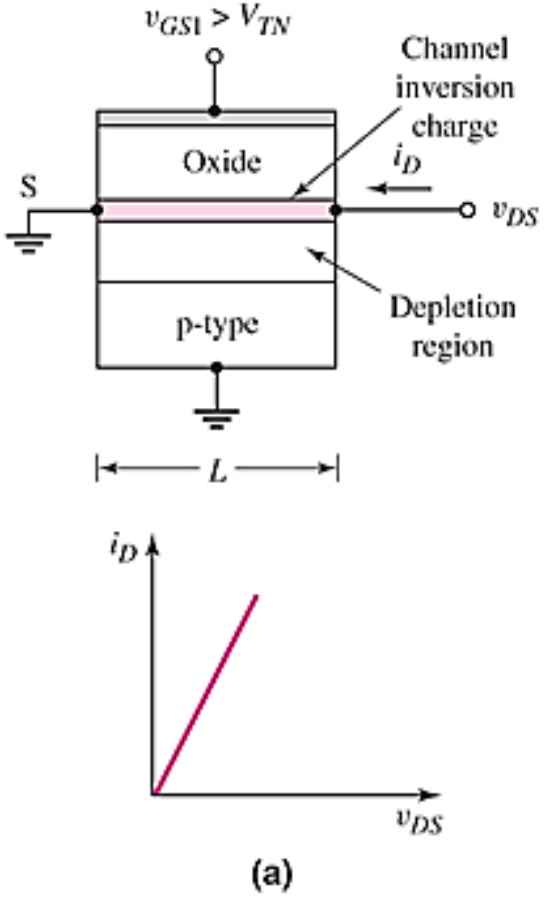
- **The i_D versus v_{DS} characteristics <u>for small values of v_{DS}</u>**

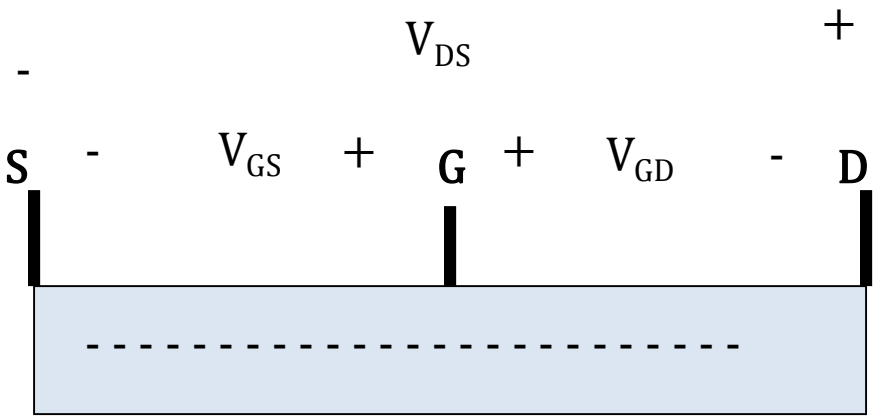
  - When $v_{GS} < V_{TN,}$ the drain current is zero.
  - When $v_{GS} > V_{TN,}$ the channel inversion charge is formed and the drain current increases with v_{DS}
  - With a larger gate voltage, a larger inversion charge density is created, and the drain current is greater for a given value of v_{DS}



Ideal MOSFET Current-Voltage Characteristics – NMOS Device

- In the basic MOS structure for $v_{GS} > V_{TN}$ with a small v_{DS}
  - The thickness of the inversion channel layer qualitatively indicates the relative charge density.
  - Which for this case is essentially constant along the entire channel length.





$V_{GS} = V_G - V_S$

$V_{GD} = V_G - V_D$

But $\mathbf{V_{GD} = V_{GS} - V_{DS}}$

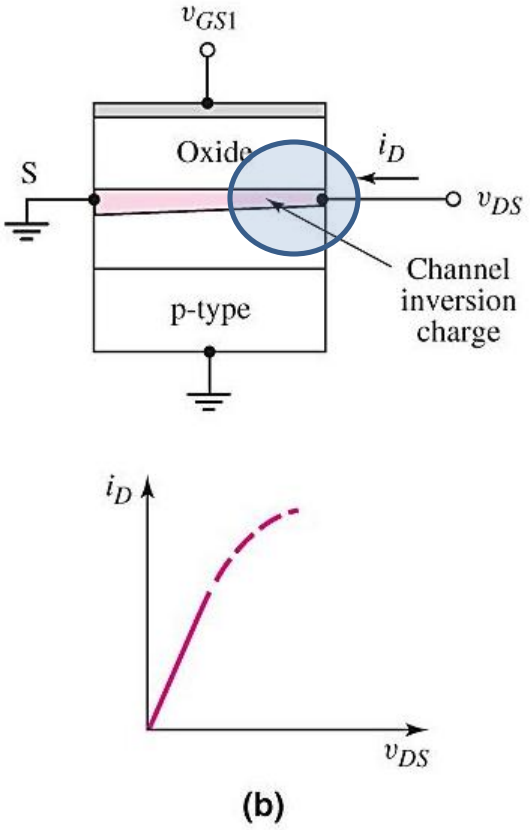
$V_{GD} = V_G - V_S - V_D + V_S$

So, if V_{DS} is small, $V_{GD} \cong V_{GS}$, we have approximately equal distribution of channel inversion layer

Ideal MOSFET Current-Voltage Characteristics – NMOS Device

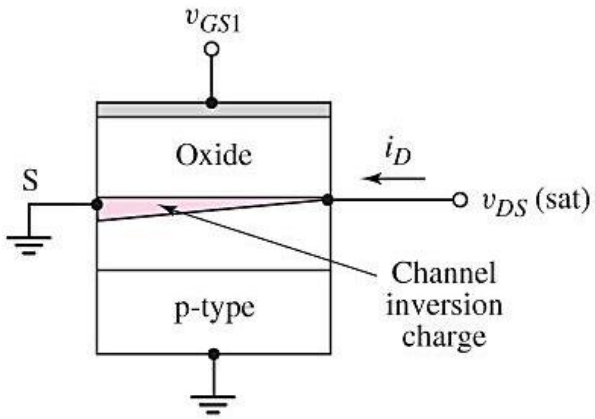
$$V_{GD} = V_{GS} - V_{DS}$$

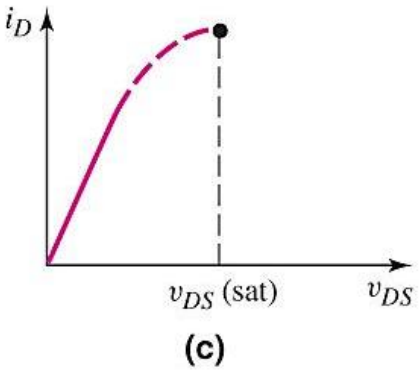
- When the drain voltage v_{DS} increases, the voltage drop across the oxide near the drain terminal decreases – no longer uniform distribution.
- It means that the induced inversion charge density near the drain also decreases.
- It causes the slope of the i_D versus v_{DS} curve to decrease.



As V_{DS} increases, the channel at the drain end reaches the pinch-off point and the value of V_{DS} that causes the channel to reach this point is called saturation voltage V_{DSsat}

$$V_{GD} = V_{GS} - V_{DS\ sat}$$





At the pinch off point, $V_{GD} = V_{TN}$

$V_{GD} = V_{GS} - V_{DS\ sat}$

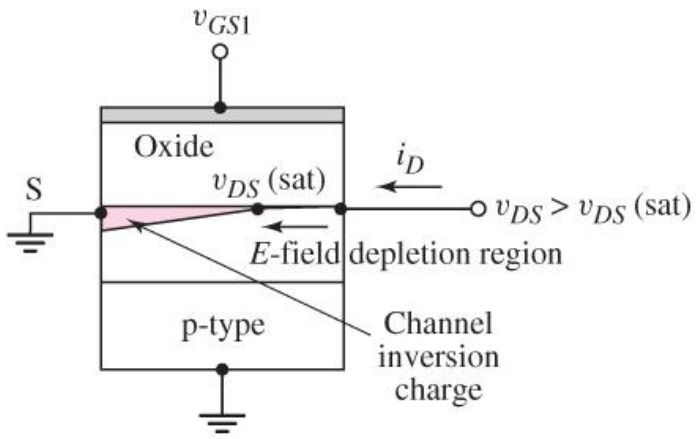
$V_{TN} = V_{GS} - V_{DS\ sat}$

Hence,

$$V_{DSsat} = V_{GS} - V_{TN}$$

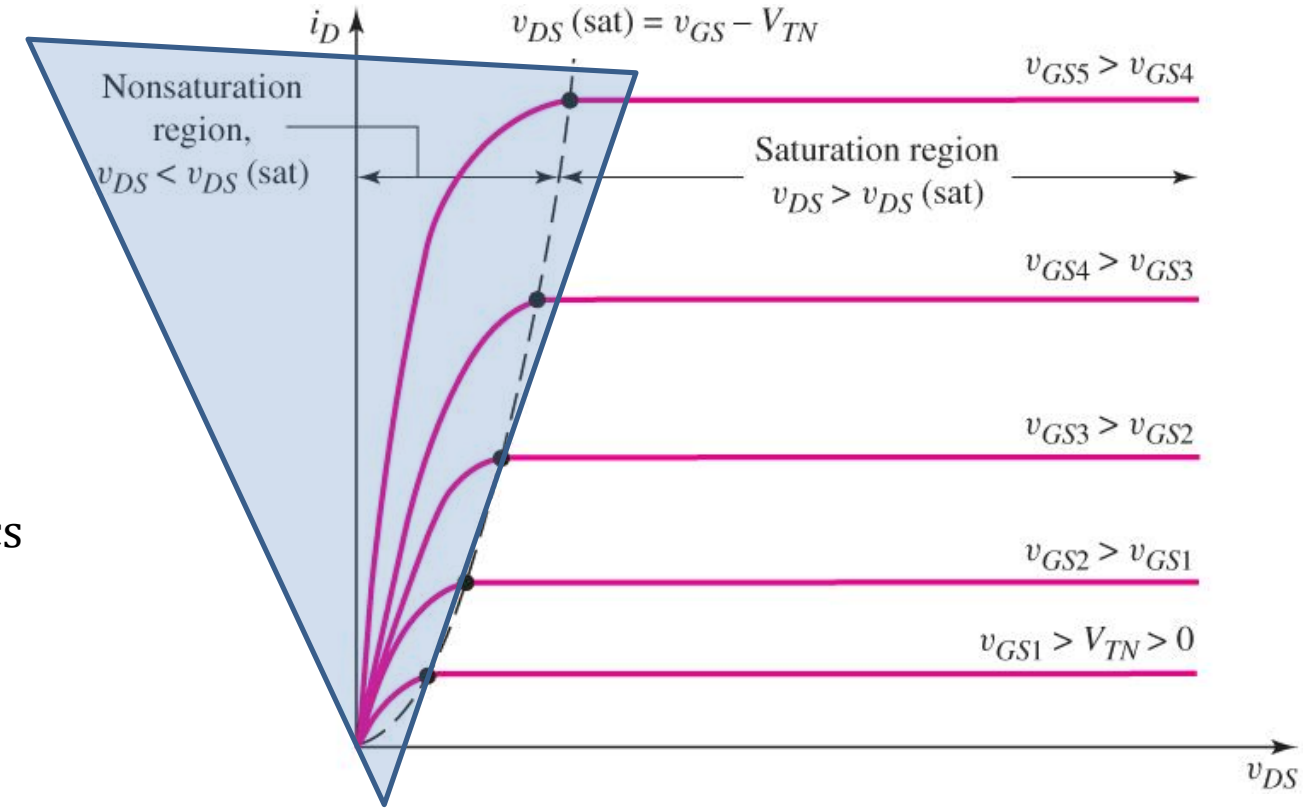
Ideal MOSFET Current-Voltage Characteristics – NMOS Device

- When v_{DS} becomes larger than v_{DS}(sat), the point in the channel at which the inversion charge is zero moves toward the source terminal.
- In the ideal MOSFET, the drain current is constant for $v_{DS} > v_{DS}$(sat).
- This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region.**
- The <u>electrons travel through the channel towards the drain but then they are swept by the electric field to the drain contact</u>



Ideal MOSFET Current-Voltage Characteristics – NMOS Device

- The region for which $v_{DS} < v_{DS}(\text{sat})$ is known as the **non-saturation** or **triode region**.
- The ideal current-voltage characteristics in this region are described by the equation:



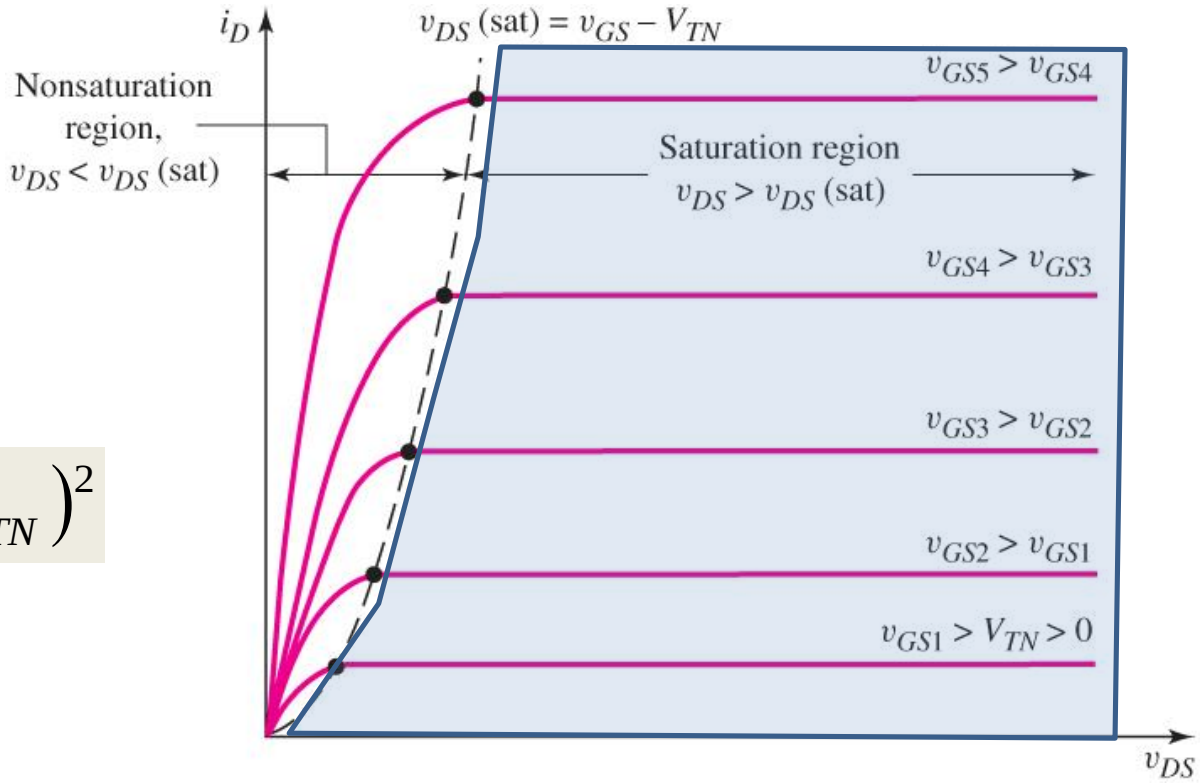
$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^{\,2}]$$

K_n = conduction parameter $\quad K_n = \dfrac{k'n}{2} \cdot \dfrac{W}{L}$

Ideal MOSFET Current-Voltage Characteristics – NMOS Device

- In the saturation region, the ideal current-voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation:

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2$$



LIST OF FORMULAS: NMOS

TRIODE OR NON-SATURATION REGION

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^{\ 2}]$$

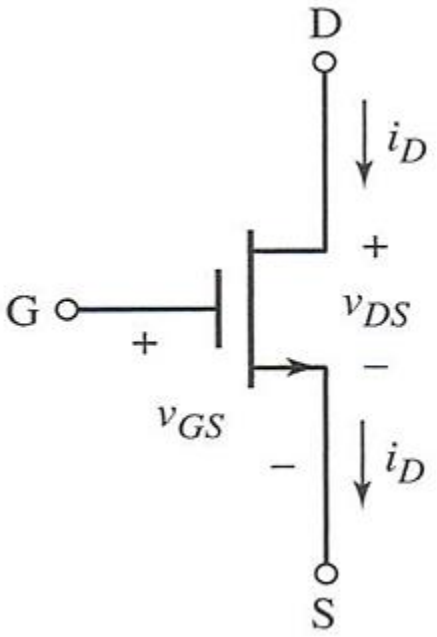
SATURATION REGION

$$I_D = K_n(V_{GS} - V_{TN})^2 \quad \text{and} \quad V_{DSsat} = V_{GS} - V_{TN}$$

Where

$$K_n = \frac{k'n}{2} \cdot \frac{W}{L}$$

Circuit Symbols and Conventions – NMOS



FET is a voltage controlled device meaning the voltage V_{GS} determines the current flowing, I_D

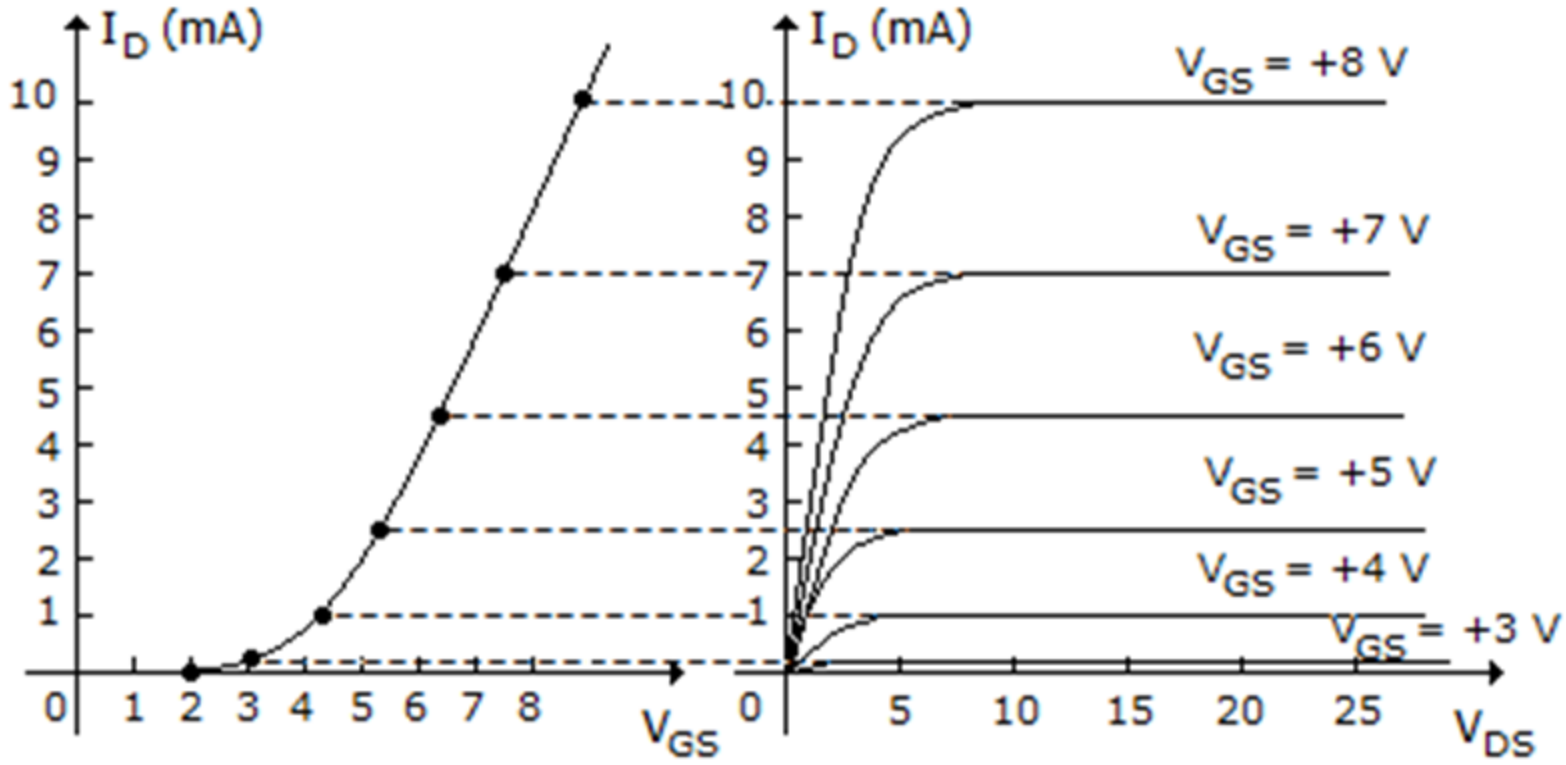
- **NMOS**
  - V_{TN} is POSITIVE
  - $V_{GS} > V_{TN}$ to turn on
  - Triode/non-saturation region

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

  - Saturation region

$$I_D = K_n(V_{GS} - V_{TN})^2$$

  - $V_{DSsat} = V_{GS} - V_{TN}$


I_D (mA)
10
9
8
7
6
5
4
3
2
1
0
1
2
3
4
5
6
7
8
V_{GS}
I_D (mA)
V_{GS} = +8 V
V_{GS} = +7 V
V_{GS} = +6 V
V_{GS} = +5 V
V_{GS} = +4 V
V_{GS} = +3 V
0
5
10
15
20
25
V_{DS}