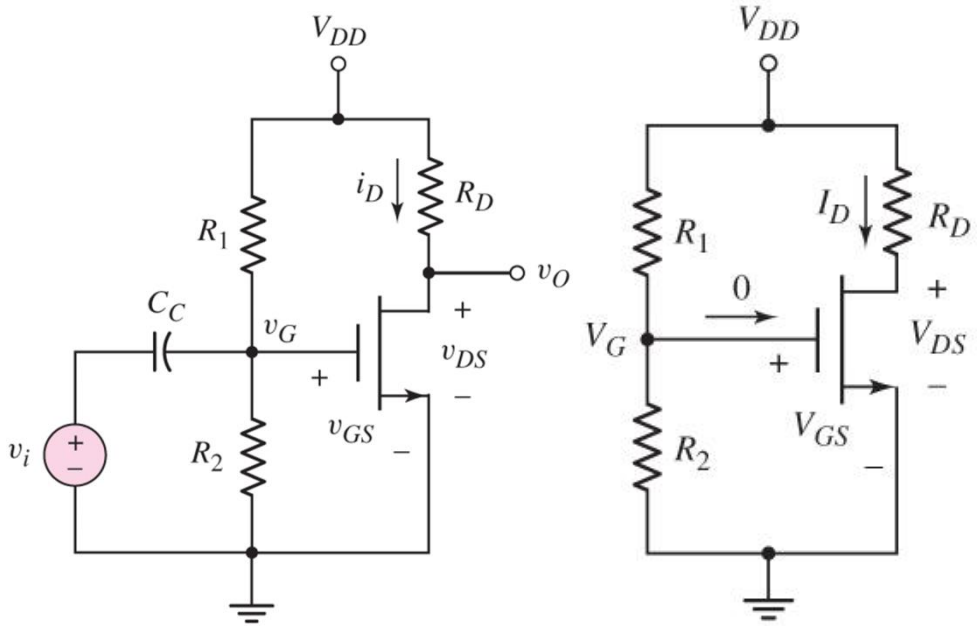
DC Analysis of FET

MOSFET DC Circuit Analysis - NMOS

- The source terminal is at ground and common to both input and output portions of the circuit.
- The C_C acts as an open circuit to dc but it allows the signal voltage to the gate of the MOSFET.



- In the DC equivalent circuit, the gate current into the transistor is zero, the voltage at the gate is given by a voltage divider principle:

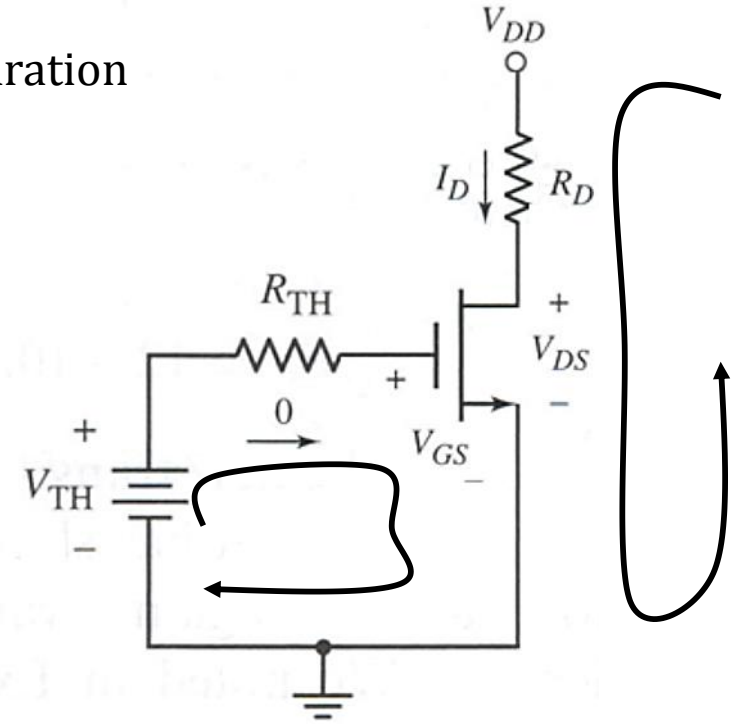
$$V_G = V_{TH} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

MOSFET DC Circuit Analysis - NMOS

1. Calculate the value of V_{GS}

2. Assume the transistor is biased in the saturation region, the drain current:

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2$$



3. Use KVL at DS loop

$$I_D R_D + V_{DS} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

4. Calculate $V_{DSsat} = V_{GS} - V_{TN}$

5. Confirm your assumption:

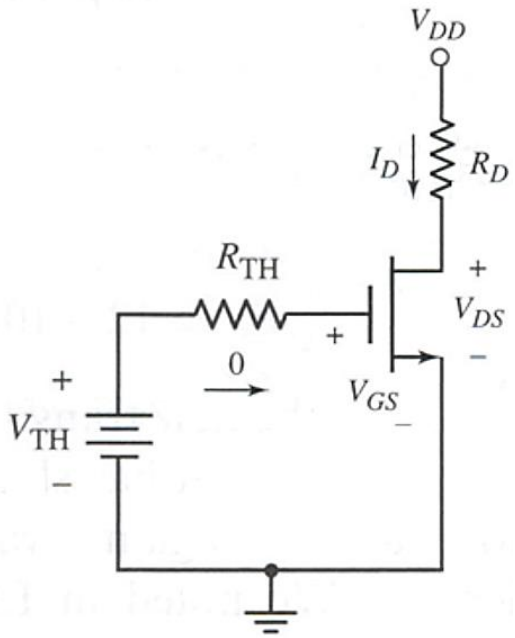
If $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$, then the transistor is biased in the saturation region. If $V_{DS} < V_{DS}(\text{sat})$, then the transistor is biased in the non-saturation region.

EXAMPLE:

Calculate the drain current and drain to source voltage of a common source circuit with an n-channel enhancement mode MOSFET. Assume that $R_1 = 30\ k\Omega$, $R_2 = 20\ k\Omega$, $R_D = 20\ k\Omega$, $V_{DD} = 5V$, $V_{TN} = 1V$ and $K_n = 0.1\ mA/V^2$

1. Calculate the value of V_{GS}

$$V_{TH} = \left(\frac{20}{30+20}\right) 5 = 2V \text{ hence } V_{GS} = V_{TH} = 2V$$



2. Assume the transistor is biased in the saturation region, the drain current:

$$I_D = K_n(V_{GS} - V_{TN})^2$$
$$I_D = 0.1(2-1)^2 = 0.1mA$$

3. Use KVL at DS loop

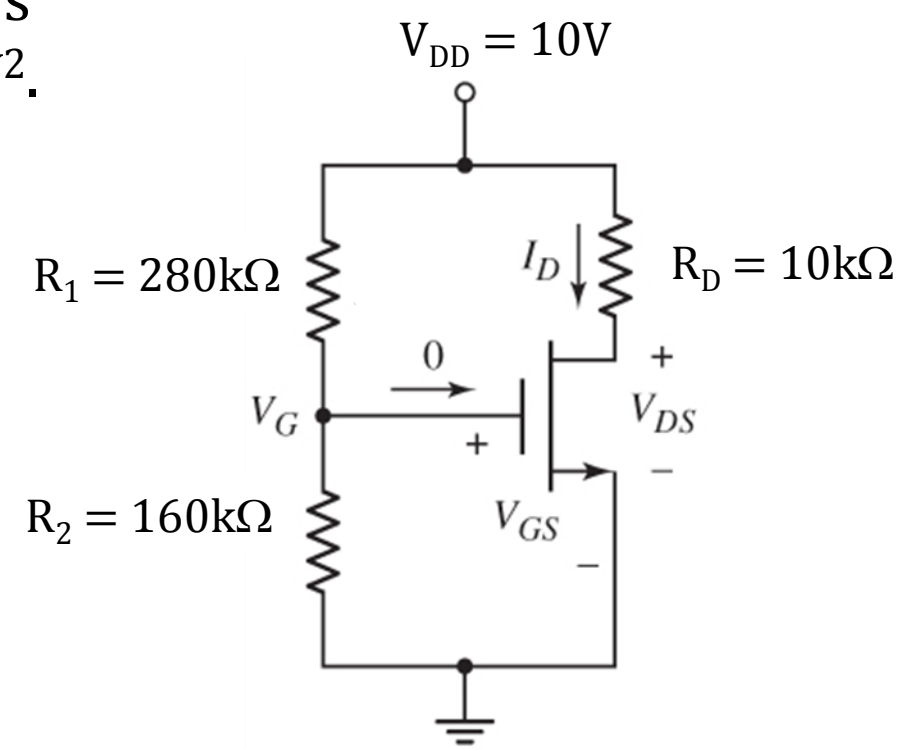
$$I_D R_D + V_{DS} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D = 3\ V$$

4. Calculate $V_{DSsat} = V_{GS} - V_{TN} = 2 - 1 = 1V$
5. Confirm your assumption: $\mathbf{V_{DS} > V_{DSsat}}$, our assumption that the transistor is in saturation region is correct

EXAMPLE

- The transistor has parameters $V_{TN} = 2V$ and $K_n = 0.25mA/V^2$.
- Find I_D and V_{DS}



Solution

1. Calculate the value of V_{GS}

$$V_{TH} = \left(\frac{160}{160 + 280}\right) 10 = 3.636\ \text{V}$$

KVL at GS loop: $V_{GS} - V_{TH} + 0 = 0 \rightarrow V_{GS} = V_{TH}$

2. Assume the transistor is biased in the saturation region, the drain current:

$$I_D = K_n (V_{GS} - V_{TN})^2$$
$$I_D = 0.25(3.636 - 2)^2 = 0.669mA$$

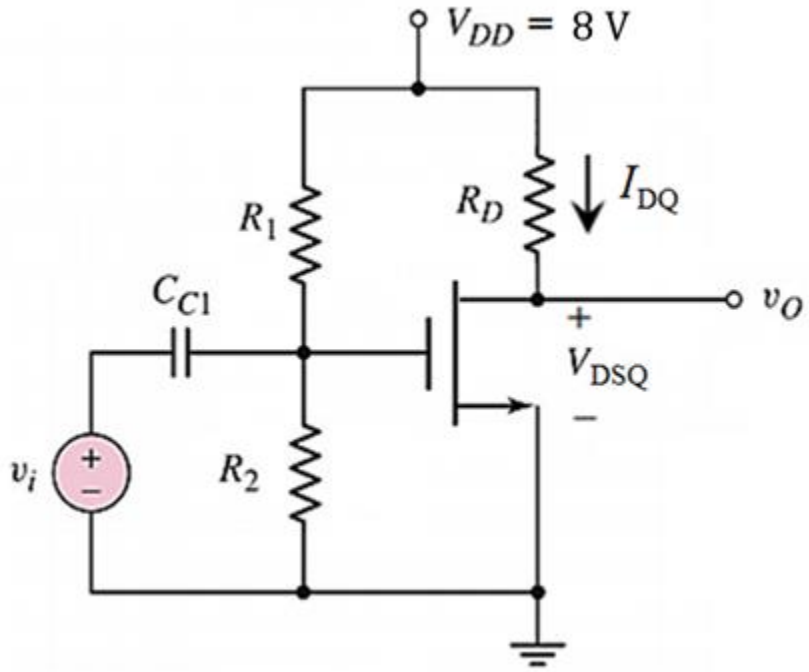
3. Use KVL at DS loop

$$I_D R_D + V_{DS} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D = 3.31\ \text{V}$$

5. Confirm your assumption: $V_{DS} > V_{DSsat}$, our assumption that the transistor is in saturation region is correct

Answer: $I_D = 0.669$ mA and $V_{DS} = 3.31$ V



The MOSFET in the circuit shown has parameters, $V_{TN} = 0.8\ V$ and $K_n = 0.03$ mA/V^2. Assume that, $R_1 = 160$ kΩ, $R_2 = 520$ kΩ and $R_D = 6$ kΩ . Calculate I_{DQ} and V_{DSQ} .

Solution

1. Calculate the value of V_{GS}

   KVL at GS loop: $V_{GS} - V_{TH} + 0 = 0 \rightarrow V_{GS} = 6.12\ V$

2. Assume the transistor is biased in the saturation region, the drain current:

$$I_D = K_n(V_{GS} - V_{TN})^2$$
$$I_D = 0.03(6.12 - 0.8)^2 = 0.85mA$$

3. Use KVL at DS loop

   $I_D R_D + V_{DS} - 8 = 0$

   $V_{DS} = 8 - 6(0.85) = \mathbf{2.9\ V}$

4. Calculate $V_{DSsat} = V_{GS} - V_{TN} = 6.12 - 0.8 = \mathbf{5.32\ V}$

5. Confirm your assumption: $\mathbf{V_{DS} < V_{DSsat}}$, our assumption that the transistor **is in saturation region is NOT CORRECT**

That means our transistor is in non-saturation mode: Go back to step 2

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$$I_D = 0.03\left[2\,(5.32)\,(8 - 6I_D) - (8 - 6I_D)^2\right]$$

$$33.33\, I_D = \left[10.64\,(8 - 6I_D) - (64 - 96I_D + 36I_D^2\right]$$

$$33.33\, I_D = \left[85.12 - 63.84\, I_D - 64 + 96I_D - 36I_D^2\right]$$

$$36\, I_D^2 + 1.17\, I_D - 21.12 = 0$$

$I_D = 0.75$ mA

$I_D = -0.78$ mA ✗

3. Go back to DS loop

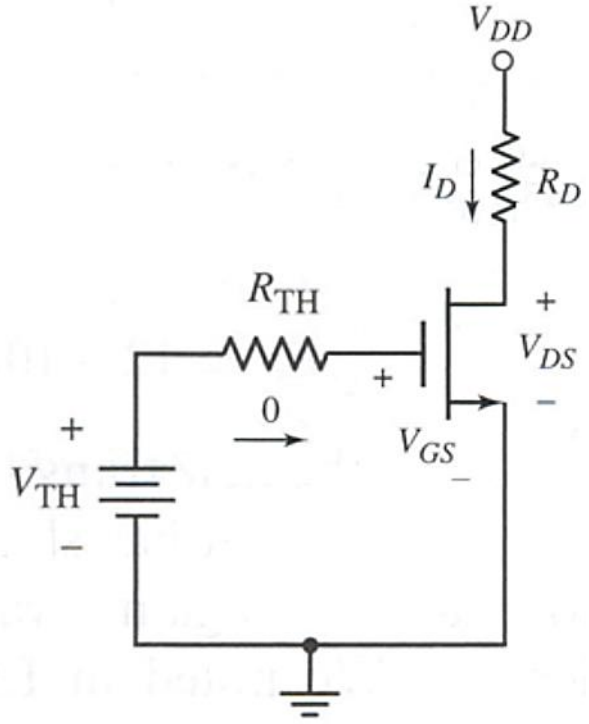
$$I_D R_D + V_{DS} - 8 = 0$$

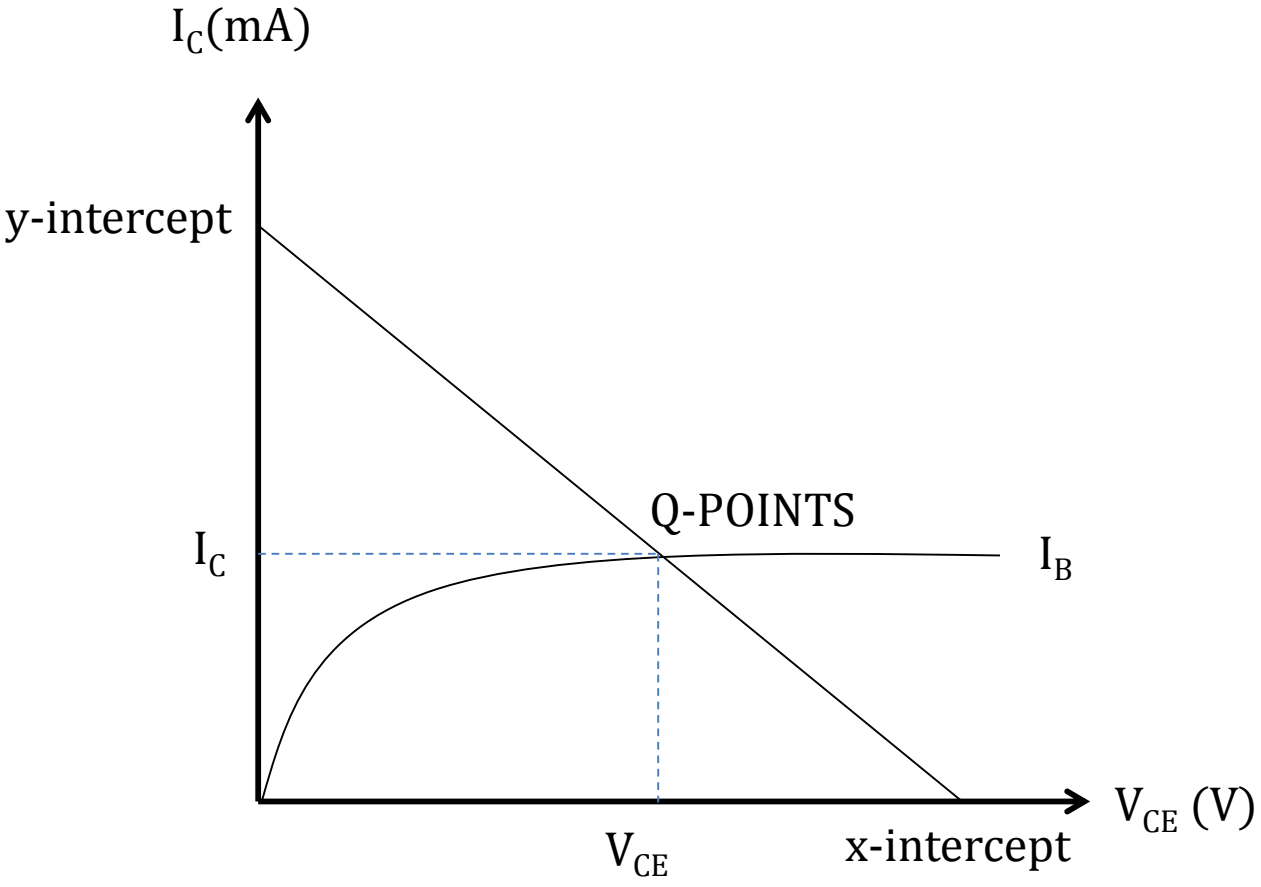
$$V_{DS} = 8 - 6(0.75) = \mathbf{3.5\ V}$$

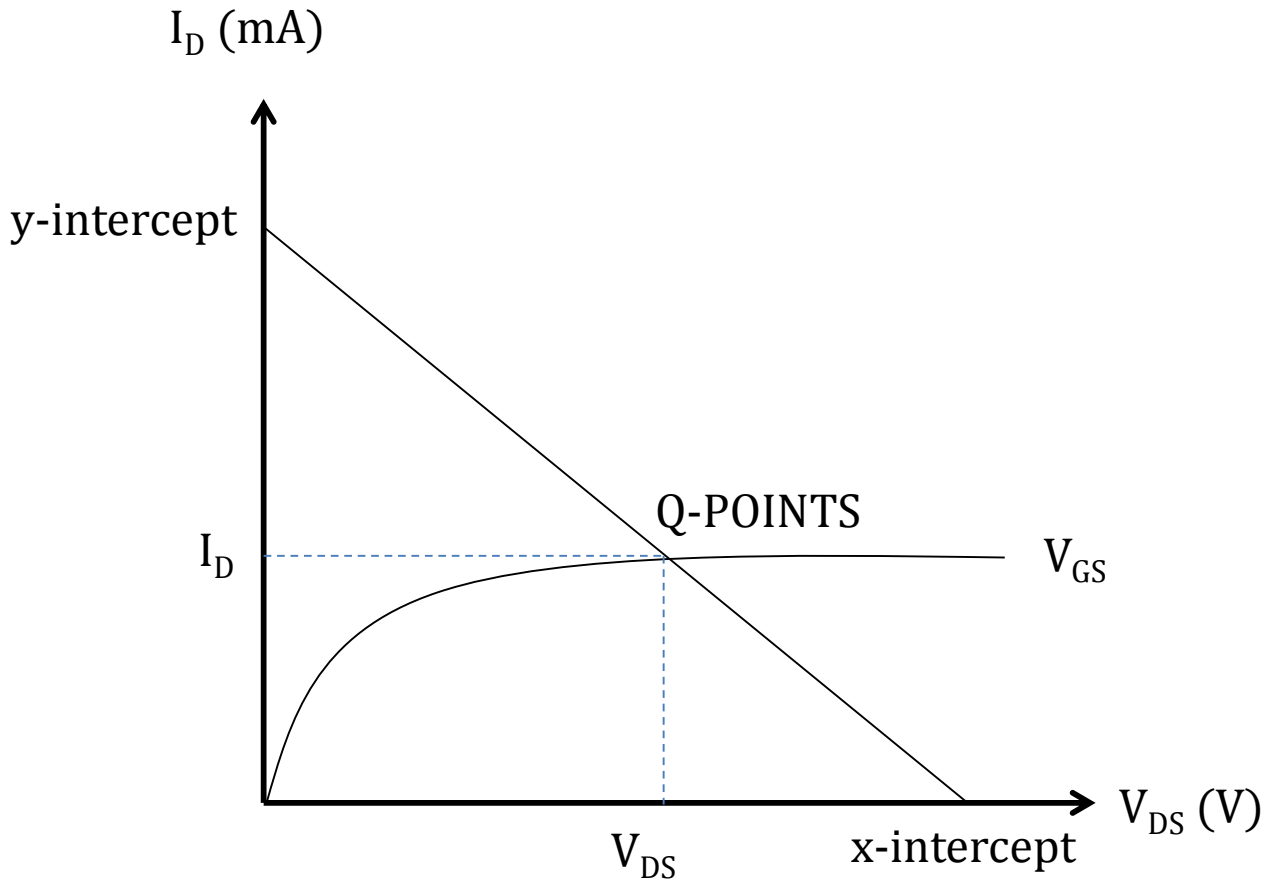
Answer: $I_D = 0.75$ mA and $V_{DS} = 3.5$V

LOAD LINE, I_D versus V_{DS}

- Common source configuration i.e source is grounded.
- It is the linear equation of I_D
- Use KVL
- $V_{DS} = V_{DD} - I_D R_D$
- $I_D = \frac{-V_{DS}}{R_D} + \frac{V_{DD}}{R_D}$

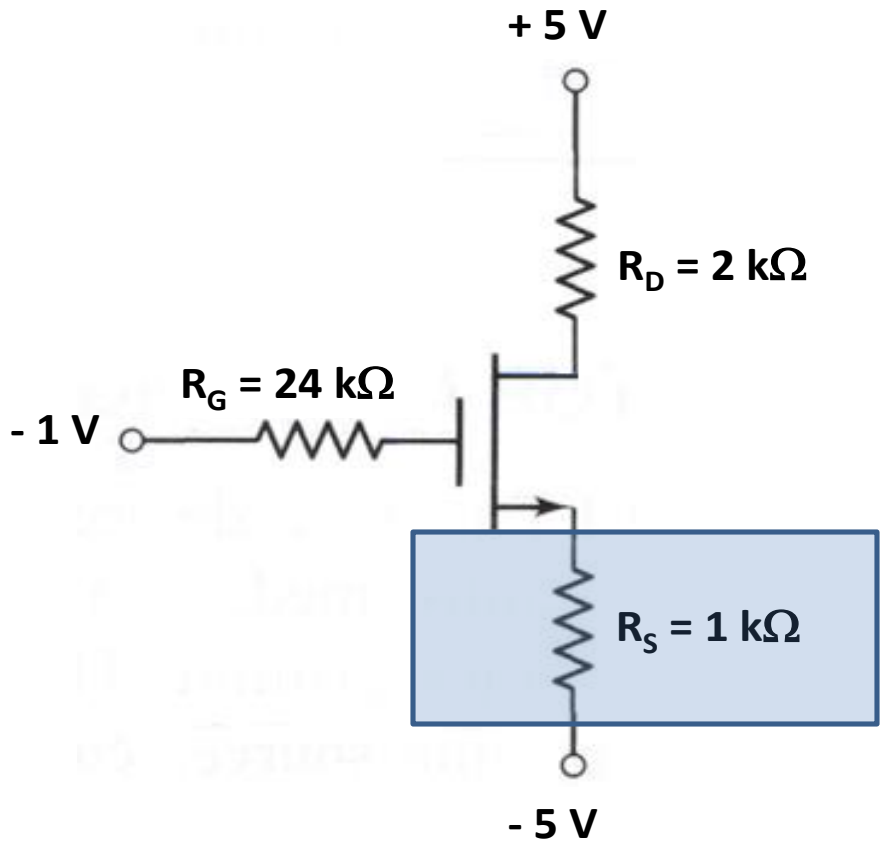



I_C(mA)
y-intercept
Q-POINTS
I_C
I_B
V_{CE} (V)
V_{CE}
x-intercept


I_D (mA)
y-intercept
Q-POINTS
I_D
V_{GS}
V_{DS} (V)
V_{DS}
x-intercept

- DC Analysis where source is NOT GROUNDED

For the NMOS transistor in the circuit below, the parameters are $V_{TN} = 1V$ and $K_n = 0.5\ mA/V^2$.



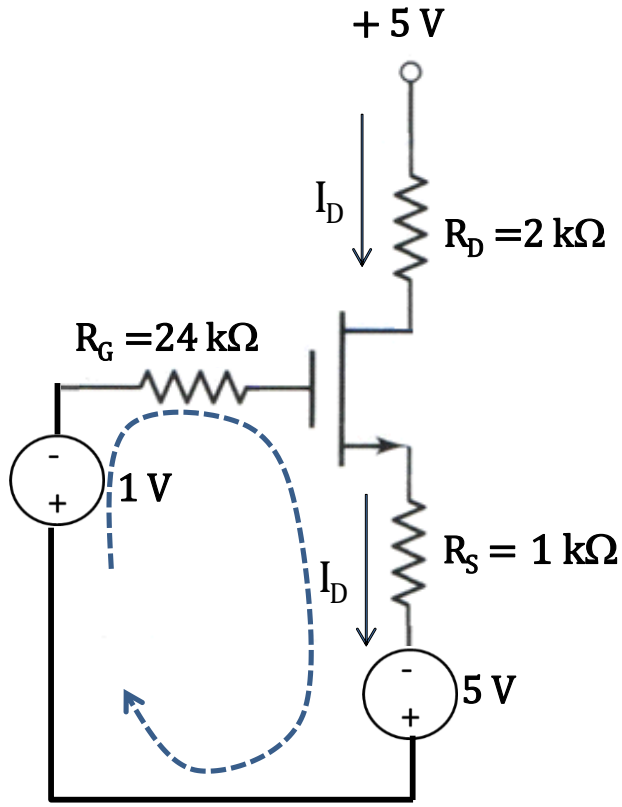
1. Calculate the value of V_{GS}

KVL at GS loop:

$$0 + V_{GS} + 1(I_D) - 5 + 1 = 0$$
$$V_{GS} = 4 - I_D$$

2. Assume the transistor is biased in the saturation region, the drain current:

$$I_D = K_n(V_{GS} - V_{TN})^2$$
$$I_D = 0.5(4 - I_D - 1)^2 = 0.5(3 - I_D)^2$$
$$2I_D = 9 - 6I_D + I_D^2$$
$$I_D^2 - 8I_D + 9 = 0$$



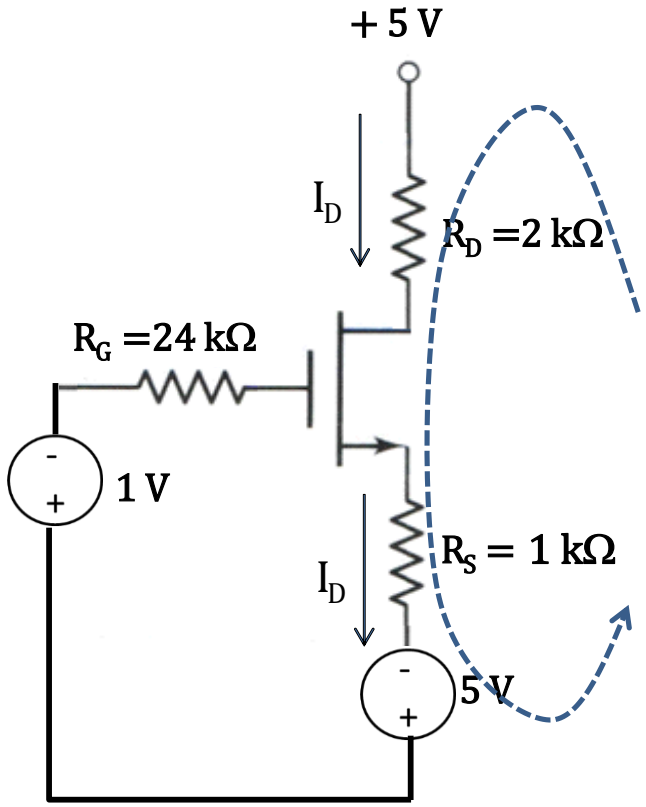
$I_D = 6.646$ mA → Replace in V_{GS} equation in step 1 $V_{GS} = 4 - I_D$ → $V_{GS} = -2.646$ V ~~(crossed out)~~

$I_D = 1.354$ mA → Replace in V_{GS} equation in step 1 $V_{GS} = 4 - I_D$ → $V_{GS} = 2.646$ V

Why choose $V_{GS} = 2.646$ V ?
Because it is bigger than V_{TN}

3. Use KVL at DS loop

$$I_D R_D + V_{DS} + I_D R_S - 5 - 5 = 0$$
$$1.354\,(2) + V_{DS} + 1.354 - 10 = 0$$
$$V_{DS} = 10 - 1.354 - 2.708 = \mathbf{5.938\ V}$$

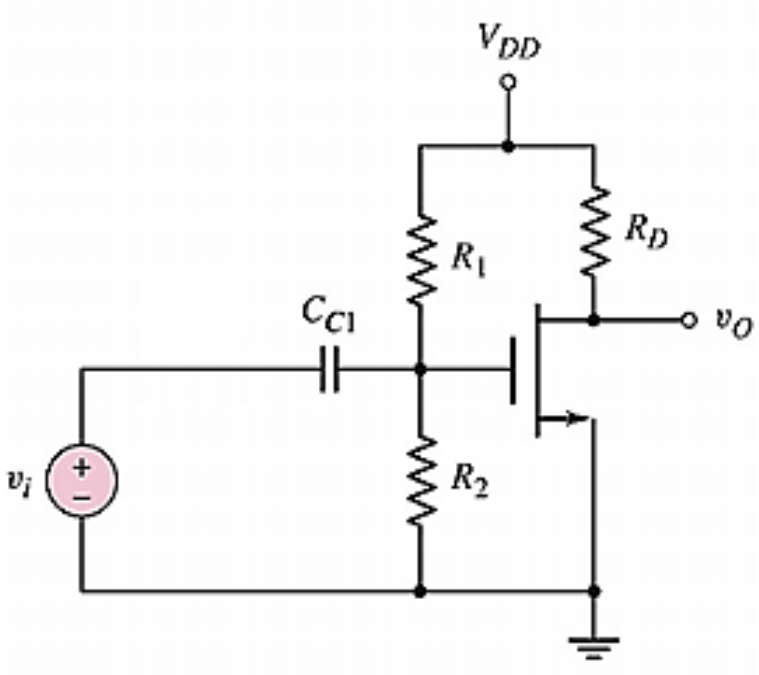


4. Calculate $V_{DSsat} = V_{GS} - V_{TN} = 2.646 - 1 = \mathbf{1.646\ V}$

5. Confirm your assumption: $\mathbf{V_{DS} > V_{DS\,sat}}$, our assumption is correct

EXAMPLE 2

Assume that the transistor parameters are V_{TN} = 0.8 V and K_n = 0.80 mA/V^2. Given V_{DD} = 5V and R_1+ R_2 = 670 kΩ, design the circuit such that I_D = 0.88 mA and V_{DS} = 2.5 V. Confirm any assumptions you make during your analysis.



Answers:
R_1 = 422 kΩ
R_2 = 248 kΩ
R_D = 2.84 kΩ